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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,663	09/20/2000	Shigeyuki Ueda	ROH-026	5545

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EXAMINER
COLEMAN, WILLIAM D

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/665,663	Applicant(s) UEDA, SHIGEYUKI	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *30 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7 and 10-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,5,7 and 10-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 30, 2002 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Idaka et al., U.S. Patent 5,587,337 in view of Eldridge et al., U.S. Patent 6,032,356.

4. Idaka discloses a semiconductor device substantially as claimed. See **FIGS. 1-12**, where Idaka teaches a semiconductor chip adapted for electrical connection to an external terminal, comprising:

a semiconductor chip body **1** having a surface with internal wiring 12 disposed thereon,

at least one surface area of the internal wiring defining a external connection pad facing in a same direction as the surface of the semiconductor chip body;

a wire connecting portion fabricated from a metal material 3/85 having oxidation resistance and electrically connected to the external connection pad 14;

a surface protective film covering the internal wiring and the surface of the semiconductor chip body while contacting the wire connecting portion in a surrounding manner such that a segment of the wire connecting portion projects from the surface protective film. However, Idaka fails to teach a wire electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal. Eldridge teaches a wire electrically connected to the segment of the wire connecting portion for connecting the semiconductor chip to the external terminal. See FIGS. 3C where Eldridge teaches a wire connection. In view of Eldridge, it would have been obvious to one of ordinary skill in the art to incorporate the wire connection portion of Eldridge into the Idaka semiconductor device because this enables the semiconductor dies to be tested and/or burned-in (Abstract, 2nd sentence).

5. Claims 2, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Idaka et al., U.S. Patent 5,57,337 and Eldridge et al., U.S. Patent 6,032,356 as applied to claim 11 above, and further in view of Kawakita et al., U.S. Patent 5,734,199.

6. Pertaining to claim 2, Idaka discloses a semiconductor device substantially as claimed as discussed above, however, Idaka fails to teach wherein the semiconductor chip is overlapped with and joined to a surface of another solid device in a state where the surface protective film is opposed to a surface of the solid device. Kawakita teaches a semiconductor device wherein the surface protective film is opposed to a surface of the solid device. See **FIG. 1** of Kawakita, where Kawakita discloses a semiconductor chip **120** (lower device) having a protective layer

115/125 is overlapped with and joined to a surface of another solid device **110** (upper device). In view of Kawakita, it would have been obvious to one of ordinary skill in the art to incorporate the device of Kawakita into the Idaka device because a first functional element is formed with first testing electrodes (Abstract, 1st sentence).

7. Pertaining to claim 3, Idaka fails to teach an internal connection pad which is partially exposed from the surface protective film in a portion different from the external connection pad, and a bump formed in a raised state on the internal connection pad. Kawakita teaches forming an internal connection pad partially exposed from the surface protective film in a portion different from the external connection pad. See **FIG. 1** of Kawakita, where internal connection pads **113** are located in a different portion than the external connection pads **124**. In view of Kawakita it would have been obvious to incorporate the location of the external connection pads in a different portion of the surface protection film of Idaka so that the semiconductor device can be tested using test electrodes (see Abstract).

8. Pertaining to claim 4, Idaka fail to disclose a solid device, which includes another semiconductor chip. Kawakita teaches interfacing another chip on top of a semiconductor chip. In view of Kawakita, it would have been obvious to incorporate another semiconductor chip on top of a semiconductor chip for LSI technology (column 1, lines 1-24).

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Idaka et al., U.S. Patent 5,587,337 and Eldridge et al., U.S. Patent 6,032,365 as applied to claim 11 above, and further in view of Hayashida et al., U.S. Patent 6,060,768.

10. Idaka discloses a semiconductor device substantially as claimed, however, Idaka fails to teach that the wire connecting portion is composed of the same material as that for the bump

(gold). Hayashida teaches a semiconductor device wherein the wire connection portion is the same material as the bump (gold). See column 14, lines 5-8 and column 15, line19 where Hayashida teaches using a bump and wire of the same material. In view of Hayashida, it would have been obvious to one of ordinary skill in the art to incorporate the same oxidation resistance wire to an oxidation resistance bump in the Idaka device, because it is well known that the connection of similar materials have excellent adhesion characteristics.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

12. Claims 7, 10 and 12 are rejected under 35 U.S.C. 102(a) as being anticipated by Nakamura Tomohito, Japanese Patent Abstract Publication 2000-234904.

13. Pertaining to claim 12, Tomohito discloses a semiconductor device having a chip-on-chip structure in which a secondary chip is overlapped with and joined to a primary chip, wherein said chip comprises

a primary chip body having a surface with internal wiring disposed thereon, at least one surface area of the internal wiring defining an external connection pad and at least one other surface area different from the at lest one surface area of the internal wiring defining an internal connection pad, both the external connection pad and the internal connection pad facing in a same direction as the surface of the primary chip body;

a wire connection portion fabricated from a metal material having oxidation resistance and electrically connected to the external connection pad;

a electrical contact projection fabricated from a metal material having oxidation resistance and electrically connected to the internal connection pad, the electrical contact projection operative to electrically connect the primary and secondary chips together; and

a surface protective film covering the internal wiring and the surface of the primary chip body while contacting the wire connecting portion and the electrical contact projection in a surrounding manner such that a segment of the wire connecting portion and a segment of the electrical contact projection from the surface protective film.

14. Pertaining to claim 7, Tomohito discloses the semiconductor chip according to claim 12, wherein said wire connecting portion is composed of the same material as that for said electrical contact projection.

15. Pertaining to claim 10, Tomohito discloses the semiconductor chip according to claim 12, further comprising a lead frame and a bonding wire, the bonding wire electrically interconnecting the lead frame and the wire connecting portion.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7721 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Examiner
Art Unit 2823

WDC
November 14, 2002